JOURNAL of CHARACTERIZATION

https://jcharacterization.com
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Journal of Characterization
Vol 3, no 3, pp.95-102, December 2023

ISSN: 2757-9166
Research Article

High-Performance Copper Oxide-Based Heterojunction Bipolar Transistor: Design, Modeling, and Performance Analysis

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(Received date: 29.11.2023 and Accepted date: 29.12.2023)

(**DOI: 10.29228/JCHAR.73922**)

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CITE : Milad Yousefizad, Samira Rezaei, Amirmohammad Shahriyari, Mohammad Mahdi Ghezelayagh, Shiva Houshmand, Negin Manavizadeh,“ High-Performance Copper Oxide-Based Heterojunction Bipolar Junction Transistor: Design,Modeling, and Performance Analysis” *JCharacterization*, vol. 3, no. 3, pp 95-102, December, 2023, doi:10.29228/JCHAR.73922

This study was presented as an oral presentation at the 3rd International Symposium on Characterization, held in Istanbul between 6-8 September 2023.

Abstract

The goal of this study is to elucidate the step-by-step process of incorporation of a Cu_2O confinement layer in an oxide semiconductor-based heterojunction bipolar to explore its impact on gain enhancement. The emitter and collector layers consist of CuO. The material of the base layer is silicon, with a confinement layer with Cu_2O added between the emitter and base regions. The transistor is designed as a PNP structure and uses the inherent characteristics of copper oxide as a p-type, which means ion-implant is a high-temperature process, so removing it and fabricating the organic subtract will be conceivable. The research involved the simulation of transistors with and without a Cu_2O confinement layer using state-of-the-art semiconductor processing techniques. Simulation results exemplify that proposed the potential barrier caused by the confinement layer prevents the electrons from moving from the base to the emitter layer. The improvement in injection efficiency caused the increase in DC gain. In SILVACO, device parameters, such as doping profile, dimensions, and material properties, were considered and modeled. Finally, the result was as the AC gain escalated to 52dB, the cut-off frequency achieved was 12 GHz, and by considering a wide range of base-emitter voltages the DC gain became >1000. This transistor with an AC gain of 52dB has applications as an audio and radio frequency amplifier and oscillator that generates a periodic waveform, it is useful in signal processing circuits, communication systems, and sensor applications to utilize in sensor circuits to amplify signals from sensors.

Keywords: Copper Oxide-based Heterojunction Bipolar Transistor, confinement layer, Injection efficiency

1. Introduction

The ever-increasing demand for smaller, faster, and more energy-efficient electronic devices has prompted intense research into novel materials and transistor designs. In this context, copper oxide-based heterojunction bipolar transistors (CuO_x-HB-Ts) have emerged as a promising solution, offering the potential for both high performance and low power consumption. Originating in 1947 as a result of fundamental research into solid-state physics conducted at Bell-Telephone Laboratories, this technology commenced its transition into the 1050s, gradually supplanting vacuum tubes. Eventually, it gave rise to the integrated circuit and microprocessor, which have become the central component of the semiconductor industry [1],[2]. Transistors are fundamental to modern electronics, acting as switches or amplifiers for electrical signals [3],[4]. They play a pivotal role in devices ranging from smartphones to computers, enabling the processing, storage, and transmission of information [5],[6].

The continual quest for smaller, faster, and more efficient transistors has driven innovation in the field. Traditional silicon-based transistors have been the workhorse of the semiconductor industry for decades. However, as electronic devices become more compact and energy-efficient, silicon-based transistors have been the workhorse of the semiconductor industry for decades. However, as electronic devices become more compact and energy-efficient, silicon-based transistors face limitations. These include power consumption concerns, heat generation, and physical size constraints that impede further miniaturization [7]. To overcome these challenges and continue the trajectory of Moore's Law researchers have been investigating alternative materials and transistor designs, Copper oxide, with its unique properties, has emerged as a promising candidate for next-generation transistors.

Recently, transition series for different applications such as transistors, solar cells, gas sensors, optical sensors and etc are used [8-16]. Copper (II) oxide (CuO) is a remarkable transition metal oxide known for its intricate interplay between various physical properties, including spin, charge, orbital, and vibrational characteristics. This material has garnered substantial attention, particularly as a p-type semiconductor [17] and a material suitable for extensive photodetection applications on a substantial scale [18]. Heterojunction Bipolar Junction Transistors (HB-JTs) is a specific type of transistor that combines the advantages of both bipolar junction transistors (BJTs) and heterojunction transistors. This hybrid design allows for precise control of electrical current flow, making it suitable for high-speed and high-frequency applications [19].

In this article, we investigate the enhancement of bandgap tunability and the introduction of impurity doping during the deposition of copper oxide. While previous research has predominantly focused on utilizing copper oxide as a channel in thin-film transistor (TFT) configurations, our study takes a different approach by employing copper oxide as the channel material in Heterojunction Bipolar Transistors (HBTs) [20-23]. We meticulously examine and evaluate the performance analysis, both in terms of AC and DC characteristics, of this specific model. To conduct our analysis, we harnessed SILVACO, a two-dimensional semiconductor simulation package, to investigate energy band diagrams, carrier distributions, and the DC and high-frequency behaviors of the system. The primary aim of this article is to enhance financial returns by introducing an extra layer of confinement. This strategic addition has been proposed with the intention of optimizing existing processes and systems, ultimately leading to increased revenue generation and improved overall profitability. By incorporating this additional confinement layer, the article seeks to capitalize on innovative approaches, harnessing the potential for higher efficiency and cost-effectiveness. The exploration of this method represents a significant step forward in the pursuit of financial growth and market competitiveness. Through meticulous analysis and experimentation, the article endeavors to demonstrate the substantial impact that this strategic enhancement can have on the overall economic performance of businesses and industries. It is anticipated that the findings presented in this article will not only contribute valuable insights to the existing body of knowledge but also offer practical solutions for businesses aiming to maximize their profits and establish a strong foothold in the market.

2. Structure

The design of the device drew inspiration from the p-CuO/n-Si/p-Cu-O heterojunction bipolar transistor (HBT), which featured a CuO emitter layer with a width of 0.1 and a p+ doping level of 10^{19} cm^{-3}, a Si base layer with a width of 0.1 and an n+ doping level of 10^{19} cm^{-3}, and a CuO collector layer with a width of 0.8 and a p+ doping level of 10^{19} cm^{-3} (Table 1) [8],[23],[25]. To enhance the amplification capability, an additional layer has been introduced into the configuration of Device A. This supplementary layer possesses a wider bandgap compared to the emitter layer, consequently elevating the potential barrier for the majority carriers within the base. The configuration under scrutiny is referred to as "Device B" (Figure 1), and exhibits variations in its layer properties. Specifically, the CuO emitter layer has a reduced thickness of 0.02 and maintains a p+ doping level of 10^{19} cm^{-3}, while the Cu_2O confinement layer also has a thickness of 0.02 and a p+ doping level of 10^{19} cm^{-3}. The Si base layer, on the other hand, has a thickness of 0.08 and is n+ doped at 10^{19} cm^{-3}. Finally, the CuO collector layer maintains its 0.8 thickness and a p+ doping level of $10^{10}cm^{-3}$(Table 2).

Table 1: Detailed Structure of Device A

Device A	Width	p+	Substance	n+
Emitter Layer	0.1	10^{19} cm^{-3}	CuO	-
Base Layer	0.1	-	Si	10^{19} cm^{-3}
Collector Layer	0.8	10^{19} cm^{-3}	CuO	-

Table 2: Detailed Structure of Device B

Device B	Width	p+		n+
Emitter Layer	0.1	10^{19} cm^{-3}	CuO	-
Base Layer	0.08	-	Si	10^{19} cm^{-3}
Collector Layer	0.8	10^{19} cm^{-3}	CuO	-
Confinement Layer	0.02	10^{19} cm^{-3}	Cu_2O	-

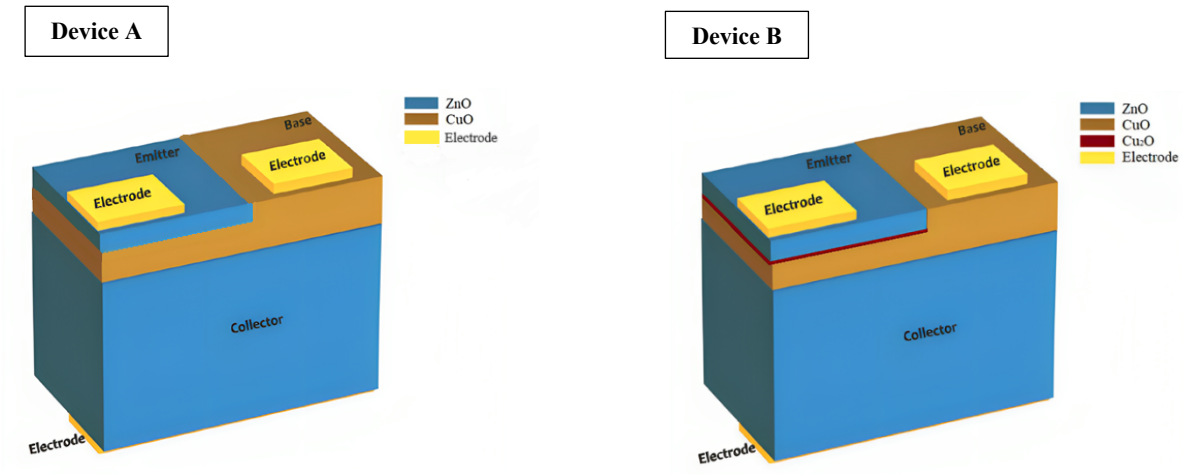

Figure 1: 3D Schematic illustration of Devices A and B

3. Results and Discussion

To generate a precise energy band diagram for device B in thermal equilibrium, it is customary to depict the energy levels of electrons in the material. This diagram serves to illustrate the organization of these energy levels within the material, offering insight into their arrangement.

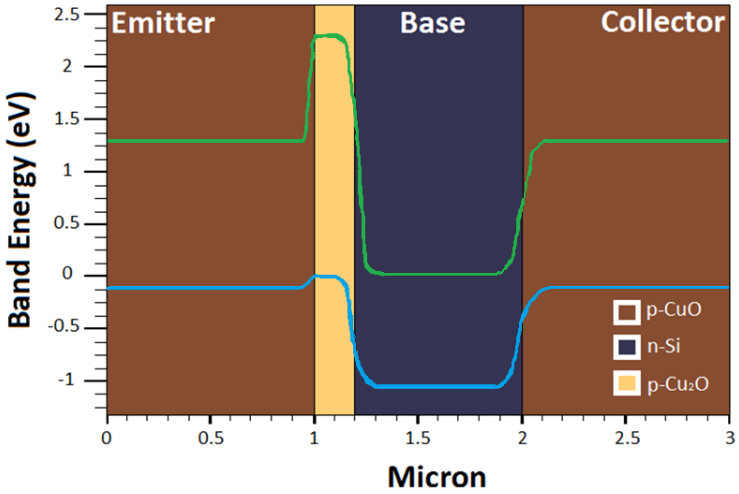

Figure 2. Energy band diagram of device B in thermal equilibrium state

Figure 2 illustrates the energy band diagram of Device B in its thermal equilibrium state. In this configuration, the introduction of a thin Cu_2O layer with a wider bandgap plays a crucial role. This layer effectively restricts the flow of electrons from the base to the emitter, resulting in enhanced device efficiency as per equation 1. Notably, in the valence band, both the E-B and C-B junction regions exhibit spike potentials of 0.1 eV and 0.12 eV, respectively. A pertinent point of comparison between Device B and Device A is that Device A features a lower spike potential.

$$\alpha_0 = \frac{I_{CP}}{(I_{EP}+I_{EN})} \qquad \text{Equation 1}$$

In the case of Device B, there exists a barrier in the conduction band that effectively hinders the flow of injected electrons from transitioning from the base into the emitter region, this barrier, located within the conduction band serves as the primary faction contributing to the heightened efficiency observed in the device, resulting in as augmented current gain, as equation 1 suggests.

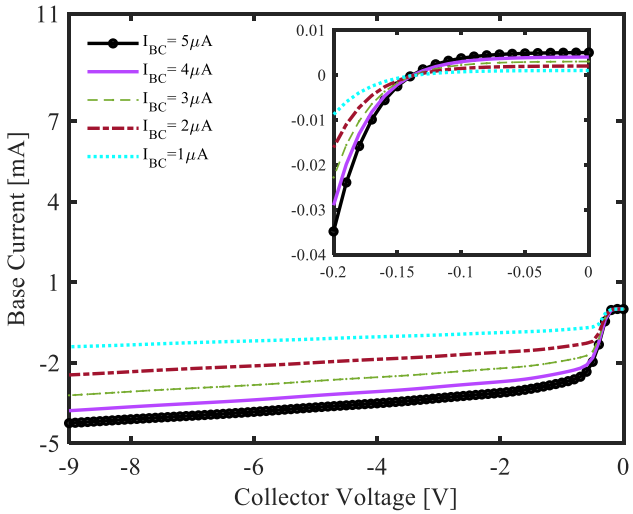

Figure 3. The current-voltage characteristic curve, the base current step is 1μA, and the inset shows the current-voltage characteristic in the common bias emitter of device B.

The collector current versus collector voltage characteristic curve for Device B is graphically depicted in Figure 3. This curve provides valuable insights into the device's operational behavior. Notably, the breakdown voltage, VBCEO (Voltage between the Collector and the Emitter with the Base Open), is measured at 2.6 V, indicating the maximum collector-emitter voltage the device can handle while maintaining its functionality. Furthermore, the base current scale on this graph is finely calibrated at one microampere, allowing for a precise examination of the

base current's influence on the collector current. One crucial parameter highlighted in Figure 3 is the turn-on voltage, which, in the case of Device B, is notably low at 0.44 V. This value represents the threshold voltage required to initiate the transistor's operation, where it transitions from an off-state to an active state, allowing current to flow from the collector to the emitter. This low turn-on voltage indicates the device's ability to swiftly respond to input signals and demonstrates its suitability for applications where rapid switching and amplification are paramount. It underscores the efficiency and versatility of Device B in various electronic circuit configurations, particularly those demanding precise control and minimal power consumption.

The inset of Figure 3 indicates the Voltage-Current characteristic curve in the common bias emitter configuration of Device B provides a more detailed view of the transistor's performance under specific operating conditions. In this configuration, the base current is incrementally stepped at a fixed value of 1μA, allowing for a systematic exploration of the transistor's behavior as the input current to the base terminal varies. This fine-grained analysis reveals critical information about the transistor's amplification capabilities and its ability to control current flow, As the base current is modulated, the transistor responds by adjusting its collector current accordingly. This dynamic relationship between the input and output currents forms the foundation of transistor-based amplification. The zoomed image enables a closer examination of key operational points, such as the threshold for turning the transistor on and the linear region where small variations in the base current yield proportionate changes in the collector current. Engineers and researchers can use this data to precisely tailor the transistor's performance to suit specific applications, ensuring optimal signal amplification and control. It's a valuable tool for designing circuits that require accurate voltage-current characteristics and reliable transistor behavior.

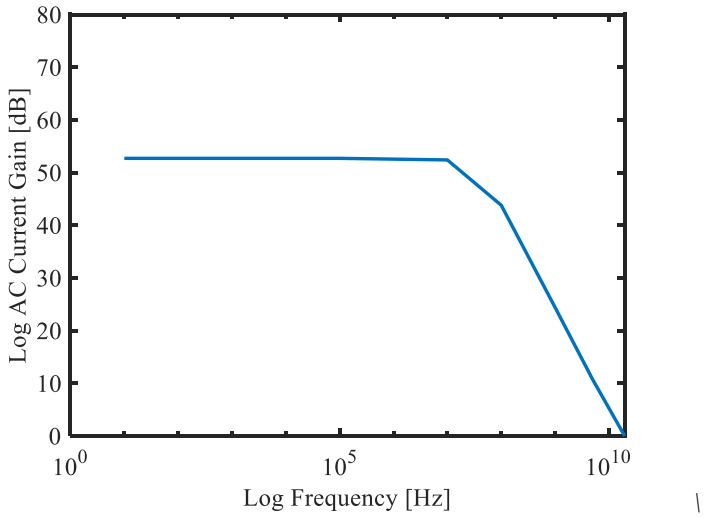

Figure 4: The device B's cut-off frequency (ft) indicates its current gain.

Figure 4 provides a comprehensive view of the performance characteristics of Device B, focusing on two vital parameters: the cut-off frequency and the AC gain. The cut-off frequency, as illustrated in the graph, is a critical metric that quantifies the upper limit of the device's operational frequency range. For Device B, this crucial value is measured at an impressive 12 gigahertz (GHz) when the collector-emitter voltage (VCE) is maintained at 1 volt. This high cut-off frequency suggests that the transistor is exceptionally capable of swiftly responding to high-frequency input signals, making it well-suited for applications requiring rapid signal processing and amplification, such as in communication systems and high-frequency electronics.

In addition, Figure 4 also provides insight into the AC gain of Device B, which is notably high at 52 decibels (dB). The AC gain represents the amplification factor that the transistor imparts to an input signal within its operational frequency range. A gain of 52 dB signifies a substantial increase in the signal's magnitude, underlining the device's prowess in signal amplification. This high AC gain is instrumental in ensuring that weak input signals are boosted to desirable levels, which is crucial for applications where signal fidelity and strength are paramount. In summary, Figure 4's depiction of the cut-off frequency and AC gain emphasizes the exceptional performance capabilities of Device B, positioning it as a valuable component in high-frequency and signal-sensitive electronic systems.

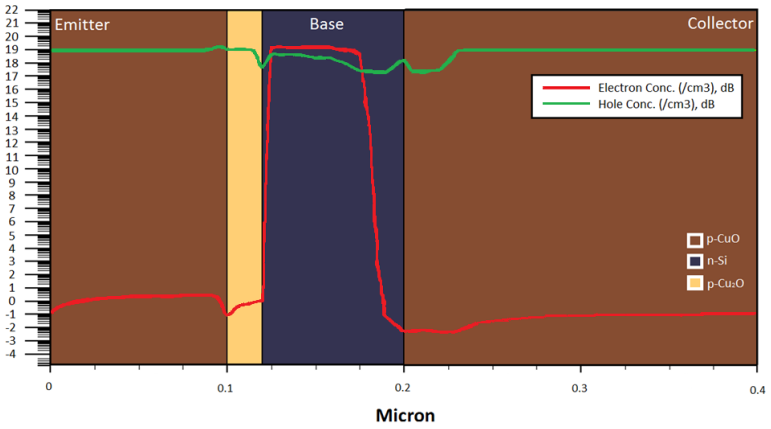

Figure 5: Density of electrons and holes in the device B within the three distinct regions of the transistor

Figure 5 demonstrates a detailed glimpse into the distribution of electrons and holes within the three distinct regions of the transistor: the emitter, base, and collector. Notably, the presence of a blocking layer composed of Cu2O within the device architecture plays a pivotal role in shaping this electron and hole distribution. This blocking layer serves as a formidable barrier, effectively preventing the injection of electrons from the base region into the emitter. This action has a profound impact on the transistor's performance, notably increasing the efficiency of the emitter. As a direct consequence of this enhanced efficiency, the transistor exhibits a substantial boost in its AC gain. In essence, Figure 5 underscores how the strategic integration of a Cu2O blocking layer within the transistor's structure can lead to significant improvements in its operational efficiency and signal amplification capabilities, making it a valuable asset in advanced electronic systems requiring precise control and enhanced performance.

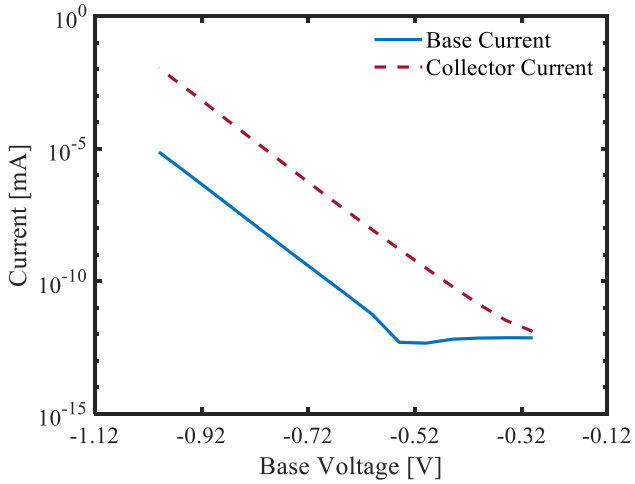

Figure 6: Gummel plot for base and collector currents of device B while base and collector are short-circuited.

The plotted diagram in Figure 6, which illustrates the relationship between base and collector currents for Device B, provides valuable insights into the transistor's operational characteristics. Notably, this device exhibits an impressive maximum collector current capacity, reaching up to 1000µA. This high collector current capability is indicative of the transistor's robust performance and suitability for applications demanding significant current amplification.

Another noteworthy aspect revealed by the diagram is the nearly ideal coefficient observed over a wide range of base voltages, governing the relationship between base and collector currents. This coefficient, approximately equal to one, signifies a highly linear and predictable behavior in the transistor's current amplification capabilities. Such linearity is crucial in many electronic applications where precise control and predictable behavior are essential.

4. CONCLUSION

This study successfully investigated the integration of a Cu_2O confinement layer in an oxide semiconductor-based heterojunction bipolar transistor, with a particular focus on its impact on gain enhancement. Through meticulous simulation using advanced semiconductor processing techniques, it was demonstrated that the incorporation of the Cu_2O confinement layer effectively raised the potential barrier, preventing undesirable electron movement from the base to the emitter layer. This improvement in injection efficiency resulted in a significant increase in DC gain. The comprehensive analysis conducted in SILVACO, considering various device parameters such as doping profile, dimensions, and material properties, revealed promising outcomes. The transistor exhibited remarkable performance metrics, with an AC gain reaching 52dB, a cut-off frequency of 12 GHz, and a DC gain surpassing 1000 under a wide range of base-emitter voltages. These findings position the transistor as a highly efficient audio and radio frequency amplifier and oscillator, capable of generating periodic waveforms.

The applications of this high-performance transistor extend across diverse domains, including signal processing circuits, communication systems, and sensor applications. Its utility in amplifying signals from sensors enhances its potential contribution to sensor circuits, further underlining the practical significance of the research. In essence, the elucidation of the step-by-step process and the subsequent experimental validation highlight the promising prospects of incorporating a Cu2O confinement layer for gain enhancement in semiconductor-based heterojunction bipolar transistors, opening avenues for advancements in electronic and communication technologies.

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